REMARKS/ARGUMENTS

Claims 1-24, 26-36, and 38 are currently pending in the present patent application, with claims 25 and 37 having been cancelled through the above claim amendments.

In a Final Office Action mailed April 19, 2006, the Examiner maintained his previous rejections of all pending claims over U.S. Patent No. 6,308,311 to Carmichael *et al.* (" Carmichael") and several other cited references. In the Final Office Action, the Examiner also objected to claims 10, 24, and 32 for several minor informalities and these minor informalities have been corrected in each of these claims. Claims 13, 14, and 24 were also rejected under the second paragraph of 35 U.S.C. § 112 for insufficient antecedent basis of specified term is utilized in each of these claims. Any such antecedent basis problems have been eliminated and these claims accordingly comply with the second paragraph of Section 112.

Before addressing the Examiner's rejections of the claims, the disclosed embodiments of the invention will first be discussed in comparison to the applied references in order to help the Examiner appreciate certain distinctions between the pending claims and the subject matter of the applied references. Specific distinctions between the pending claims and the applied references will be discussed after the discussion of the disclosed embodiments and the applied references. This discussion of the differences between the disclosed embodiments and applied references does not define the scope or interpretation of any of the claims.

Referring to Figure 3 of the present application, a host processor 42 may be directly coupled through a suitable industry-standard bus, such as a PCI bus or Rapid I/O format, to a pipeline circuit 80 (Figure 4) formed from a programmable logic integrated circuit (PLIC) such as an FPGA. This architecture may look structurally similar to the prior art system discussed with reference to Figure 2 of Carmichael, but in fact is very different from this prior art system as well as the system illustrated in Figure 3 of Carmichael.

In the present application, the host processor 42 may communicate directly over an industry standard pipeline bus 50 like a PCI bus to reconfigure target FPGAs 80 as shown in Figures 3 and 4. The pipeline circuit 80 of Figure 4 may be PLIC like an FPGA and when this is true the FPGA itself includes logic that performs the functions of the interfacing with the industry-standard bus 50. No external circuitry is required to form this required interface. This may reduce cost and also simplifies the overall system since no separate

interface between the host processor 42 and the FPGAs 80.

In contrast to embodiments of the present invention, Carmichael utilizes an interface device 30 as shown in Figure 3 that is separate from a target FPGA 10. The target FPGA 10 to be programmed or reconfigured is coupled through the interface device 30 to a host system 20. This block diagram illustrates the most general concept of the invention of Carmichael. Systems prior to Carmichael, as described with reference to Figure 2 of Carmichael, utilized the host system 20 to download configuration data through an interface device 15 to the target FPGA 10. In these types of systems, the interface device 15 was simply a cable and also contained an FPGA to convert a bit stream from the host system 20 into a corresponding bit stream for configuring the target FPGA 10. With the approach of the system of Figure 2, the host system 20 is primarily responsible for generating the configuration data and thus this presents a relatively heavy processing burden on the host system.

Returning now to Figure 3 of Carmichael, Carmichael's solution is to introduce the interface device 30 which offloads some of this processing burden from the host system 20. The approach of Figure 2 may be said to use a programmable device, namely the host system 20, to program the target FPGA 10. In contrast, the approach illustrated in Figure 3 of Carmichael introduces a second programmable device, namely the interface device 30, to program or offload some of the programming responsibility from the host system 20 and the interface device 30 programming the target FPGA 10. In the Carmichael system, the interface device 30 is separate from the target FPGA 10.

It should also be noted that with embodiments of the present invention, an industry-standard bus 50, such as a Rapid IO bus or PCI is used to configure the FPGAs. In addition to the address, data, and control signals for this configuration, application programs executing on the host processor 42 also communicate as well as the bus over which the target FPGA is programmed. Thus, with the approach of the present application there is no need for a separate or dedicated configuration bus to configure the FPGAs. This is in contrast to the approach of Carmichael. Carmichael shows in Figure 3 two busses, a serial or RS-232 bus 42 and a USB bus 40 through which the host system 20 is connected to the interface device 30.

While the busses 40 and 42 are industry-standard busses, in the system of Carmichael these busses are only contemplated as being configuration busses for the

target FPGA 10. In other words, the approach of Carmichael requires a dedicated configuration bus between the host system 20 and the target FPGA 10. Thus, the target FPGA 10 cannot simply be coupled to a PCI bus of the host system 20 and then programmed directly, as with embodiments of the present application. In contrast, the interface device 30 in Carmichael must be coupled through the dedicated configuration bus to the host system 20 and the target FPGA 10, in turn, connected to the interface device. Once again, while Carmichael appears at first glance very similar to the present application, the similarity, or apparent similarity is misleading and inaccurate. The present application discusses the desire to have a standard bus such as a PCI bus over which the target FPGA 10 can be programmed or reconfigured. In this way, a custom bus need not be designed for allowing the host system to reconfigure the target FPGAs. At first glance it appears that Carmichael is utilizing industry-standard busses as discussed in the present application since the standard RS-232 and USB busses are being utilized on the host system 20. But as pointed out, while these are standard busses, they are nonetheless being utilized as dedicated configuration busses in the approach of Carmichael. Thus, in Carmichael standard peripheral devices are not coupled to the busses 40 and 42.

Turning now to the claims, amended claim 1 recites a programmable circuit including a programmable logic integrated circuit that includes an interface. The interface is operable to receive multiple versions of firmware from an external source, each version of firmware representing a corresponding operating configuration, store the multiple versions of firmware in a memory, and download a selected one of the versions of firmware from the memory. Carmichael neither discloses nor suggests a programmable logic integrated circuit including an interface that operates as recited. In fact, the integration of an interface into the programmable logic integrated circuit (PLIC) was not practical at the time of Carmichael. FPGAs 10 at this time had capacities that were too small to allow integration of the functionality of the interface device 30 of Carmichael into the FPGA itself. If such circuitry was integrated into the FPGA10 itself at the time of Carmichael, the FPGA would have insufficient capacity remaining to allow for programming of the FPGA to perform the desired function. Neither does Carmichael teach or suggest including the interface into the PLIC itself. Increased capacity for PLICs means more sophisticated logic can be implemented in each PLIC, but does not render obvious the inclusion of another function, i.e., the interface of the PLIC to the processor, into the PLIC.

For these reasons, the combination of elements recited in claim 1 is allowable and dependent claims 2-6 are allowable for at least the same reasons as claim 1 and due to the additional limitations added by each of these claims. Neither do any of the other cited references disclose the recited elements of amended claim 1 and thus Carmichael and any combination of the other references of record do not render claim 1 obvious.

Independent claims 7, 10, and 13 are allowable for reasons similar to those just discussed with reference to claim 1, and the dependent claims 8-9, 11-12, and 14-15 are allowable for at least the same reasons as the associated independent claim and due to the additional limitations added by each of these claims.

Amended claim 16 recites a computing machine including a processor and an industry-standard bus coupled to the processor. The industry-standard bus is adapted to be coupled to standard peripheral devices. The machine includes a memory that stores a plurality of firmware configurations and a programmable logic integrated circuit coupled to the memory. The programmable logic integrated circuit is also coupled to the processor through the industry-standard bus and is operable to, receive from the processor a new firmware configuration that represents a new configuration of the programmable circuit, store the new firmware configuration in the memory, and download the new firmware configuration from the memory in response to the processor.

Claim 16 recites the programmable logic integrated circuit is coupled to the processor through the industry-standard bus. The industry-standard bus is adapted to be coupled to standard peripheral devices. Carmichael neither discloses nor suggests such a structure. The industry-standard busses in Carmichael are not being used as conventional busses but as dedicated configuration busses. Thus, standard peripheral devices would not be coupled to these busses in Carmichael. Neither do any of the other cited references disclose the recited elements of amended claim 16 and thus Carmichael and any combination of the other references of record do not render claim 16 obvious.

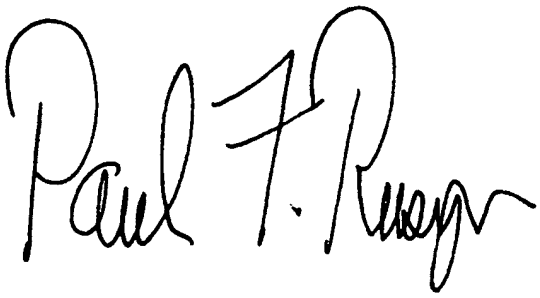
For these reasons, the combination of elements recited in amended claim 16 is allowable and dependent claims 17-19 are allowable for at least the same reasons as claim 16 and due to the additional limitations added by each of these claims. The remaining independent claims are allowable for reasons similar to those set forth above with regard to claims 1 and 16 and each of the remaining dependent claims is allowable for at least the same reasons as the associated independent claim and due to the additional

limitations added by that claim.

The present patent application is in condition for allowance. Favorable consideration and a Notice of Allowance are respectfully requested. Should the Examiner have any further questions about the application, Applicant respectfully requests the Examiner to contact the undersigned attorney at (425) 455-5575 to resolve the matter. If any need for any fee in addition to that paid with this response is found, for any reason or at any point during the prosecution of this application, kindly consider this a petition therefore and charge any necessary fees to Deposit Account 07-1897.

Respectfully submitted,

GRAYBEAL JACKSON HALEY LLP



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